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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,964	08/04/2003	Kazutaka Inukai	0553-0376	5167

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EXAMINER	
LESPERANCE, JEAN E	
ART UNIT	**PAPER NUMBER**
2674	

DATE MAILED: 01/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/633,964	INUKAI, KAZUTAKA	
	Examiner	Art Unit	
	Jean E Lesperance	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/4/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 to 20 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 1-18 are rejected under 35 USC 102 (e) as being unpatentable over US Patent ~~Application~~ Pub. No. # 20020044124 ("Yamazaki et al.")

As per claim 1, Yamazaki et al. teach a plurality of pixels 104 are arranged in a matrix shape in the pixel portion Fig.3 (103) corresponding to a plurality of pixels arranged in a pixel portion, wherein each column has four or more data lines (S1 to Sx) in the pixel portion.

As per claim 2, Yamazaki et al. teach a plurality of pixels 104 are arranged in a matrix shape in the pixel portion Fig.3 (103) corresponding to a plurality of pixels arranged in a pixel portion, wherein the source signal linesFig.3 (S1 to Sx) corresponding to two or more data lines are placed in each of the plural pixels.

As per claim 3, Yamazaki et al. teach a pixel portion Fig.5 (103) comprising a switching element (201) and EL element (204) corresponding to wherein the pixels each have a switching element and a light emitting element, and wherein the switching element is connected to one of the two or more data lines, which is predetermined for each pixel.

As per claim 4, Yamazaki et al. teach a plurality of source signal lines Fig.5 (S1 to Sx) corresponding to a plurality of data lines in a column direction; a plurality of gates signal lines Fig.5 (G1 to Gy) corresponding to a plurality of scanning lines in a row direction; and a plurality of pixels 114 are arranged in a matrix shape in the pixel portion Fig.5 (103) corresponding a plurality of pixels arranged into a matrix pattern, the pixels each having a light emitting element (204), wherein x data lines (x is a natural number equal to or larger than 4) out of the plural data lines (S1 to Sx) are placed in each column and one scanning line (G1) out of the plural scanning lines is placed in each row, wherein y scanning drivers (y is a natural number equal to or larger than 1) are provided to select x scanning lines out of the plural scanning lines simultaneously, and the electric power source potential of the electric power source supply lines V1 to Vx are applied to data source lines (Fig.5 (S1 to Sx) corresponding to wherein x data drivers are provided to simultaneously supply signals to x pixels selected out of the plural pixels through the x data lines placed in each column.

As per claim 5, Yamazaki et al. teach Fig.5 (S1 to Sx) corresponding to x data lines (x is a natural number equal to or larger than 4) placed in each column; Gate line Fig.5 (G1) corresponding to one scanning line placed in each row; and a plurality of

pixels 114 are arranged in a matrix shape in the pixel portion Fig.5 (103) corresponding to a plurality of pixels placed at points where the data lines and the scanning line intersect to form a matrix pattern, the pixels each having a light emitting element (204), wherein y scanning drivers (y is a natural number equal to or larger than 1) are provided to select x scanning lines out of the plural scanning lines simultaneously, and the electric power source potential of the electric power source supply lines V1 to Vx are applied to data source lines (Fig.5 (S1 to Sx) corresponding to wherein x data drivers are provided to simultaneously supply signals to x pixels selected out of the plural pixels through the x data lines placed in each column.

As to claims 6 and 7, Yamazaki et al. teach a TFT having a structure in which hot carrier injection is reduced so as not to have a very large drop in operational speed is used as an n-channel TFT 503 of a CMOS circuit forming the driver circuit portion. Note that circuits such as a shift register, a buffer, a level shifter, and a sampling circuit (sample and hold circuit) are included as the driver circuits here. Signal conversion circuits such as a D/A converter can also be included when performing digital drive (page 13, lines 0196) corresponding to the x data drivers each have a plurality of shift registers and sampling circuits and the shift registers each operating independently, each of the sampling circuits being associated with one of the shift registers.

As to claims 8 and 9, Yamazaki et al. teach a TFT having a structure in which hot carrier injection is reduced so as not to have a very large drop in operational speed is used as an n-channel TFT 503 of a CMOS circuit forming the driver circuit portion. Note that circuits such as a shift register (first and second latches) , a buffer, a level

shifter, and a sampling circuit (sample and hold circuit) are included as the driver circuits here. Signal conversion circuits such as a D/A converter can also be included when performing digital drive (page 13, lines 0196) corresponding to wherein the x data drivers each have a plurality of shift registers, first latches, second latches, and sampling circuits, the shift registers each operating independently, each of the first latches, each of the second latches, and each of the sampling circuits being associated with one of the shift registers.

As per claims 10-12, Yamazaki et al. teach the EL display device is also referred to as organic EL display (OELD) or an organic light emitting diode (OLED) (page 1, lines 0006)corresponding to wherein the light emitting element comprises an OLED.

As to claims 13 and 14, Yamazaki et al. teach a source signal line driver circuit Fig.1 (101) and a gate signal line driver circuit (102) are formed on the same conductive film 105 formed on the pixel portion 103 corresponding to wherein the plural pixels, the y scanning drivers, and the x data drivers are formed on the same insulator.

As per claims 15-18, Yamazaki et al. teach a plurality of pixels 114 are arranged in a matrix shape in the pixel portion Fig.5 (103) corresponding to wherein the pixels each have a driving transistor Fig.5 (202), a switching transistor (201), and a capacitor (203), the driving transistor (202) controlling a current value of the light emitting element (204), the switching transistor (201)controlling input of a video signal into its pixel, and the capacitor (203) holding the video signal and the erasing transistor Fig.6 (504) discharging electric charges that are held in the capacitor.

3. Claims 19 and 20 are rejected under 35 USC 102 (e) as being unpatentable over US Patent ~~Application~~ Pub. No. # 2001/0035863 ("Kimura").

As for claims19 and 20, Kimura et al. teach the sustain (turn on) period Ts.sub.3 of the least significant bit portion is shorter than the address (write in) period Ta.sub.3. Therefore, as shown in FIG. 4A, if there is a transition to the address (write in) period Ta.sub.1 of the next frame period immediately after the completion of the sustain (turn on) period Ts.sub.3, a period develops in which the address (write in) periods of differing subframe periods overlap. Selection of a plurality of gate signal lines is performed simultaneously in this period, and therefore normal image display cannot be performed (Page 8, lines 0125) corresponding to wherein one frame period has a plurality of sub-frame periods, wherein the plural sub-frame periods each have a writing period and a light emission period, or a writing period, a light emission period, and an erasure period, and wherein, in the writing period, y scanning drivers (y is a natural number equal to or larger than 1) select x scanning lines simultaneously whereas x data drivers simultaneously supply signals to x pixels selected out of the plural pixels through the x data lines placed in each column (See Figure 5).

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean Lesperance whose telephone number is (703) 308-6413. The examiner can normally be reached on from Monday to Friday between 8:OOAM and 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on (703) 305-4709 .

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Jean Lesperance

Art unit 2674

Date 1/21/2005

HENRY N. TRAN
PRIMARY EXAMINER